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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,536	09/24/2004	Min-Chih Hsuan	13301-US-PA	5535

31561 7590 12/08/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,536	HSUAN ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 5-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al (6,908,784 B1).

1. Regarding claim 1, Farnworth et al discloses a wafer level chip scale package structure process, comprising: providing a glass substrate having a first surface and a second surface, wherein an interconnect pattern is disposed on the first surface of the glass substrate (Figure 8B, reference 14A); providing a wafer comprising a plurality of chips and having an active surface and a back surface (Figure 8B, reference 12), wherein a plurality of bumps is disposed on the active surface of the wafer (Figure 8B, reference 10A); flipping the wafer, so that the active surface of the wafer faces the first surface of the glass substrate (Figure 8B); disposing the wafer on the glass substrate and connecting the active surface of the wafer to the first surface of the glass substrate through attachment of the bumps and the interconnect pattern (Figure 8B); dicing the wafer (Figure 13E, reference 26); drilling the glass substrate to form a plurality of through holes; and forming a plurality of via plugs in the through holes in the glass substrate (column 18, lines 21-67); dicing the glass substrate and the interconnect pattern to form a plurality of chip scale package structures (Figure 1B, reference 26).

2. Regarding claim 5, Farnworth et al discloses wherein a redistribution layer is formed on the second surface of the glass substrate and a plurality of solder balls are formed on the second surface of the glass substrate, after dicing the glass substrate and the interconnect pattern (column 9, lines 6-17).

3. Regarding claim 6, Farnworth et al discloses wherein a wafer level testing process is performed through the via plugs or the interconnect pattern before dicing the glass substrate and the interconnect pattern (Figure 9A, reference 76A).

4. Regarding claim 7, Farnworth et al discloses wherein the via plugs are formed by plating (column 21, lines 31-45).

5. Regarding claim 8, Farnworth et al discloses wherein a material of the via plug is copper (column 9, lines 33-42).

6. Regarding claim 9, Farnworth et al discloses grinding the wafer from the back surface of the wafer before dicing the wafer (column 22, lines 47-55).

7. Regarding claim 10, Farnworth et al discloses a wafer level chip scale package structure process, comprising: providing a glass substrate having a first surface and a second surface (Figure 8A, reference 14A) providing a wafer comprising a plurality of chips that are to be separated along scribe-lines and having an active surface and a back surface (Figure 8A, reference 12), wherein a plurality of pads are disposed on the active surface of the wafer and cover a portion of the scribe-lines of the wafer (column 9, lines 17-48); flipping the wafer in order to face the active surface of the wafer to the first surface of the glass substrate and attaching the active surface of the wafer to the first surface of the glass substrate (Figure 8B); drilling the glass substrate to form a plurality of through holes and forming a plurality of via

plugs in the through holes in the glass substrate (column 18, lines 21-67); and dicing the wafer and the glass substrate along the scribe-lines to form a plurality of chip scale package structures (column 9, lines 17-48).

8. Regarding claim 11, Farnworth et al discloses wherein the glass substrate has no interconnection pattern (Figure 8A, reference 14A).

9. Regarding claim 12, Farnworth et al discloses wherein the pads are attached to the glass substrate through a thermal cured adhesive (Figure 8C, reference 36A).

10. Regarding claim 13, Farnworth et al discloses wherein a redistribution layer is formed on the second surface of the glass substrate and a plurality of solder balls are formed on the second surface of the glass substrate, after dicing the wafer and the glass substrate (column 9, lines 6-17).

11. Regarding claim 14, Farnworth et al discloses wherein a wafer level testing process is performed through the via plugs before dicing the wafer and the glass substrate (Figure 9A, reference 76A).

12. Regarding claim 15, Farnworth et al discloses removing the scribe-lines of the wafer from the second surface of the wafer by etching (column 9, lines 33-48).

13. Regarding claim 16, Farnworth et al discloses grinding the wafer from the back surface of the wafer, after attaching the active surface of the wafer to the first surface of the glass substrate (column 22, lines 47-55).

14. Regarding claim 17, Farnworth et al discloses wherein the via plugs are formed by plating (column 21, lines 31-45).

15. Regarding claim 18, Farnworth et al discloses wherein a material of the via plug is copper (column 9, lines 33-42).

16. Regarding claim 19, Farnworth et al wherein each of the via plugs is aligned to and connected to one pad (Figure 9A, reference 18A).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al (6,908,784 B1) in view of Canning et al (5,783,465).

17. Farnworth et al discloses all above claimed subject matter except the glass substrate is an indium tin oxide glass plate (claim 2), bumps attached through eutectic bonding (claim 3), and bumps are attached through anisotropic conductive film (claim 4).

Canning et al discloses the glass substrate is an indium tin oxide glass plate (column 3, lines 21-25), bumps attached through eutectic bonding (column 1, lines 31-35), and bumps are attached through anisotropic conductive film (column 3, lines 20-21).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Farnworth et al with the teachings of Canning et al for the purpose of using compliant metal coated photodefined polymer bumps for mounting and interconnecting component assemblies on glass substrates.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
December 1, 2005

CARL WHITEHEAD, JR
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800